REMARKS

In the Office Action identified above, the Examiner rejected claims 14 and 15 under 35 U.S.C. § 112, second paragraph; rejected claims 8, 14, 21 and 22 under 35 U.S.C. § 102(e) as being anticipated by Tanaka et al. (U.S. Patent No. 6,774,462 B2, "Tanaka"); rejected claims 9 and 16 under 35 U.S.C. § 103(a) over Tanaka in view of Examiner's Official Notice; and objected to claims 10, 11, 17, and 20 as being dependent upon a rejected base claim, but indicated that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.[1]

Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 10, 11, 17, and 20, as well as claims 12-13, which depend from claim 11, and claims 18-19, which depend from claim 17.

In the present Amendment, Applicants have amended claims 8, 10-11, 14-15, 17, and 21, and have added new claims 23 and 24 to protect additional aspects of the present invention. As a result, claims 1, 8-24 are pending in the above-captioned application, of which claims 8-24 are presented for examination.

New claims 23 and 24 recite a method of manufacturing a semiconductor device including, among other elements, "forming first and second stack films on the first dielectric film of the first and second regions respectively, each of the first and second stack films having a first electrode material layer, a second dielectric film having a

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[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement of characterization in the Office Action.

thickness of 5 Å or more and 100 Å or less, and a second electrode material layer, an etching rate of the first and second electrode material layers of the first stack film being different from an etching rate of the first and second electrode material layers of the second stack film." Support for new claims 23 and 24 may be found in the specification, for example, at page 8, line 13, to page 9, line 30, and Figs. 5 and 9.

Regarding the rejection of claims 14 and 15 under 35 U.S.C. § 112, second paragraph, the Examiner stated that these claims are "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." Office Action at page 2. In response, Applicants have amended claims 14 and 15 to recite "the second dielectric film." Accordingly, Applicants request that the Examiner withdraw the rejection of claims 14 and 15 under 35 U.S.C. § 112, second paragraph.

Applicants respectfully traverse the rejection of claims 8, 14, 21 and 22 under 35 U.S.C. § 102(e) as being anticipated by Tanaka. In order to properly establish that Tanaka anticipates Applicants' claimed invention under 35 U.S.C. § 102, each and every element of each of the claims in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Claim 8, for example, is not anticipated by Tanaka because the reference fails to teach each and every element of the claim. In particular, Tanaka at least fails to

disclose "forming a second dielectric film having a thickness of 5 Å or more and 100 Å or less on the first electrode material layer," as recited in amended claim 8.

The Examiner alleges that Tanaka teaches "formation of a second dielectric film 105 on the first electrode 104, wherein the second dielectric has a thickness of 50 Angstroms." Office Action at page 3. However, Tanaka discloses that element 105 in Figs. 1-5 is a *tungsten nitride* film. As generally understood, tungsten nitride is a conductive material with low resistance, not a dielectric. See Attached Article titled "Physical and Electrical Properties of Ta-N, Mo-N, and W-N Electrodes of HfO_2 High-k Gate Dielectric" and http://www.reade.com/Products/Nitrides/tungsten_nitride.html. Tungsten nitride (WN) is another film used for conductive layers. Therefore tungsten nitride film 105 of Tanaka cannot constitute the "second dielectric film having a thickness of 5 Å or more and 100 Å or less on the first electrode material layer," as recited in claim 8. Thus, claim 8 is allowable over Tanaka, and claims 14, 21 and 22 are also allowable at least due to their dependence from claim 8.

Applicants respectfully traverse the Examiner's rejection of claims 9 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Tanaka in view of Examiner's Official Notice. A *prima facie* case of obviousness has not been established.

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). M.P.E.P. § 2142, 8th Ed., Rev. 4 (October 2005), p. 2100-134.

Claims 9 and 16 depend from claim 8 and thus require each and every element recited in claim 8. A *prima facie* case of obviousness has not been established because, among other things, Tanaka and Examiner's Official Notice, taken alone or in combination, fail to teach or suggest each and every element recited in claim 8 and required by dependent claims 9 and 16. As discussed above in regard to the Examiner's 35 U.S.C. § 102(e) rejection of claim 8, Tanaka fails to teach or suggest the claimed "forming a second dielectric film having a thickness of 5 Å or more and 100 Å or less on the first electrode material layer." The Examiner's Official Notice, even if properly taken, fails to overcome the deficiencies of Tanaka. Claims 9 and 16 are therefore allowable over the combination of Tanaka and Examiner's Official Notice at least due to their dependence from claim 8.

New claim 23, while of different scope, recites features similar to those recited in claim 8. For example, claim 23 recites "a second dielectric film..." Accordingly, claim 23 is allowable at least for reasons discussed above in regard to claim 8, and claim 24 is allowable at least due to its dependence from claim 23.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: May 10, 2006

By: _____
Selah C. Park
Reg. No. 57,127

Attachments: 1) Article titled "Physical and Electrical Properties of Ta-N, Mo-N, and W-N Electrodes of HfO_2 High-k Gate Dielectric"; and
2) http://www.reade.com/Products/Nitrides/tungsten_nitride.html.

Physical and electrical properties of Ta–N, Mo–N, and W–N electrodes on HfO_2 high-k gate dielectric

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(Received 19 May 2005; accepted 12 December 2005; published 26 January 2006)

The influence of various types of metal nitride gate electrodes, i.e., tantalum nitride, molybdenum nitride, and tungsten nitride, on electrical characteristics of metal-oxide-semiconductor capacitors with hafnium oxide as the gate dielectric material has been studied. The result shows that both the physical and electrical properties of the high-k gate stack are influenced by the gate electrode materials and the post-metal-annealing temperature. Both the physical thickness and equivalent oxide thickness of the gate stack increased after the high-temperature N_2 annealing step. The leakage current density decreased with the increase of the annealing temperature from 600 to 800 °C. The work functions of these metal nitride electrodes decreased with the annealing temperature due to the variance of microstructure and chemical composition, as indicated by x-ray diffraction and second-ion-mass spectroscopy data. These metal nitride electrodes are suitable for n-channel metal-oxide-semiconductor device applications after 800 °C N_2 annealing because their work functions are between 4.05 and 4.25 eV. The interface state density and oxide trap density of the high-k gate stack were also reduced by the high-temperature N_2 annealing step. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2163683]

I. INTRODUCTION

As the gate oxide thickness scaled down below to 1.5 nm, the thermally grown SiO_2 could not serve as the gate dielectric material for complementary metal-oxide-semiconductor (CMOS) devices because of many issues, such as excessively large gate leakage current, dopant penetration from polycrystalline silicon (poly-Si) gate electrode, and reliability concerns.[1,2] Alternative high dielectric constant materials are necessary to replace thermally grown SiO_2 in the sub-0.1-μm technology node in order to reduce the leakage current and to improve the reliability because a thicker gate dielectric layer can be used. Many metal oxides, such as Ta_2O_5, HfO_2, ZrO_2, Y_2O_3, and Al_2O_3 are considered as promising candidates. Unlike thermal-grown SiO_2 gate dielectric, most high-k gate dielectric materials are not compatible with the poly-Si gate electrode, i.e., forming an interface layer at the poly-Si/high-k contact region.[3–5] The poly-Si gate also has many other disadvantages such as poly-Si gate depletion and high resistance.[6–8] Metal electrodes have been studied as replacements for poly-Si gate to solve these problems. For example, metal gate electrodes do not have the problems of poly-Si gate depletion and dopant diffusion. The metal gate electrode also has a much lower electrical resistivity.

There are many requirements for the metal gate electrode, including low electrical resistivity, high thermal stability, low reactivity, adequate work functions for p-channel or n-channel devices, and easiness to deposit and process.[9–11] Refractory metals such as Ta, W, and Mo are promising gate electrode materials. However, pure metals may have relatively poor thermal stability and high chemical reactivity at elevated temperatures.[12,13] Metal nitrides, such as tantalum nitride (Ta–N), molybdenum nitride (Mo–N), and tungsten nitride (W–N), are good diffusion barriers with low resistance and high thermal stability.[14–16] Moreover, the work functions of the metal nitrides may be adjusted with the nitrogen contents.[17–19] Therefore, metal nitrides are potentially important gate electrode materials for high-k gate dielectrics in future metal-oxide-semiconductor field-effect transistor (MOSFET) devices.

Metal nitride films may be deposited by many methods, such as metal-organic chemical-vapor deposition (MOCVD), atomic layer deposition (ALD), and physical-vapor deposition (PVD). In this study, metal nitrides were deposited by reactive sputtering because it is a simple process and can be done at a low temperature. Ta–N, Mo–N, and W–N electrodes, were ovaluated as the gate electrodes for the hafnium oxide (HfO_2) gate dielectric, which is a promising high-k gate dielectric material. The physical and electrical properties of these metal nitride films were characterized using the MOS capacitor structure, which contained an ultrathin (2.5 nm) HfO_2 film deposited by ALD. Influences of various electrode materials and process conditions were investigated.

II. EXPERIMENTAL PROCEDURES

The MOS capacitors studied in this work were fabricated using a HF-cleaned p-type (100) Si substrate (doping level $\sim 10^{17}$ cm^{-3}). The metal nitride film was sputter deposited on an ALD HfO_2 (2.5 nm thick) in two steps: (1) a thin nitrogen-rich film was deposited by sputtering the metal targets in a mixture of 50% N_2/50% Ar for 30 s, and (2) a second nitride film was deposited by sputtering the metal target in a mixture of N_2/Ar for 90 min. The optimum

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N_2/Ar flow ratio varies with the type of metal nitride. For example, for Ta–N, Mo–N, and W–N electrodes, the N_2/Ar ratios were 5%/95%, 10%/90%, and 2.5%/97.5%, respectively. The N_2/Ar gas flow ratios that correspond to the lowest metal nitride resistivities were selected.[20] The sputtering pressure was fixed at 5 mTorr. The round-shaped metal nitride gate (with a gate area of 3×10^{-4} cm^2) was deposited through a shadow mask. The gate electrodes were processed through a high-temperature annealing step in a N_2 ambient, at 10 Torr, for 10 s at 600 or 800 °C in a separate heating chamber attached to the load-lock chamber of the sputtering system. The backside SiO_2 was stripped with a dilute HF solution after the front of the wafer was covered with a positive photoresist layer. A 300-nm-thick aluminum (Al) film was then dc sputter deposited on backside Si to form the Ohmic contact. Then, the photoresist layer was stripped off with a photoresist stripper. Lastly, all the MOS capacitors were annealed in a forming gas ambient (10% H_2/90% N_2) at 300 °C for 30 min in a tube furnace. In the later discussions, the as-deposited samples are referred to the samples without the high-temperature N_2 annealing step but with the backside 300 °C Al forming gas annealing step. For the metal nitride work-function evaluation, MOS capacitors with various HfO_2 thicknesses were prepared and characterized.

The resistivities of the metal nitride films were measured with a four-point probe (Keithley DMM 196). The gate electrode/high-k interface layer structures were characterized with an energy dispersive x-ray spectroscopy (EDXS), electron-energy-loss spectroscopy (EELS), high-resolution transmission electron microscopy (HRTEM), time-of-flight secondary-ion-mass spectroscopy (TOF-SIMS), and x-ray diffraction (XRD). The electrical properties, such as equivalent oxide thickness (EOT), flatband voltage (V_{FB}), interface state density (D_{it}), and leakage current density (J) were estimated from the capacitance-voltage (C-V) and current-voltage (I-V) data, which were measured with an Agilent HP 4284A Precision LCR Meter and an Agilent HP 4155C Parameter Analyzer, respectively. The work function (Φ_m) of a metal nitride gate electrode was extracted from the V_{FB} vs EOT curve.

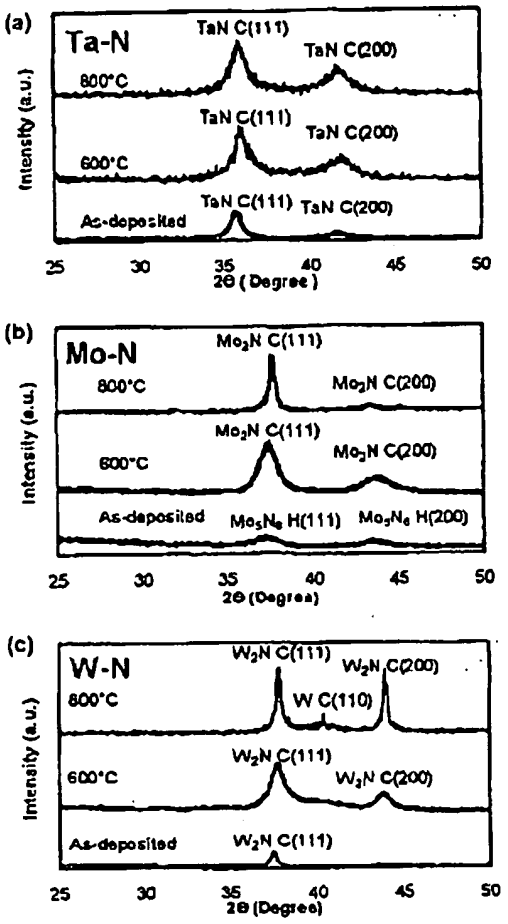

FIG. 1. X-ray-diffraction patterns of (a) tantalum nitride, (b) molybdenum nitride, and (c) tungsten nitride gate electrodes on 2.5 nm HfO_2 films with and without 10 s 600 or 800 °C N_2 annealing at 10 Torr. All the samples were also annealed in forming gas at 300 °C for 30 min after the backside Al deposition. The peaks are indexed for cubic (C) TaN (a), for cubic (C) Mo_2N, and hexagonal (H) Mo_5N_6 (b), and for cubic (C) W_2N and cubic (C) W.

III. RESULTS AND DISCUSSIONS

A. Physical properties

1. *Microstructures of gate electrodes*

The microstructures of three metal nitride gates were studied by XRD. Figure 1(a) shows the XRD patterns of the as-deposited, 600 and 800 °C N_2 annealed Ta–N films. Prominent cubic (C) TaN (111) and (200) peaks were observed in all three samples. No metallic Ta crystal phases were observed in any of these films, suggesting that the films were fully nitridized. The figures also show that the crystallinity of the Ta–N film improved with the increase of the N_2 annealing temperature. The C (200) peak became sharp and narrow after both 600 and 800 °C N_2 annealings. The increase of the TaN C (200) peak height in Fig. 1(a) implies an increase of crystallization with the increase of the annealing temperature. Separately, the SIMS result in Fig. 2 shows that the nitrogen concentration in the bulk Ta–N film increases with the N_2 annealing temperature. The nitrogen content is an important factor for the XRD peak shape. For example, it was reported that the XRD pattern of the as-deposited Ta–N films varied with the nitrogen partial pressure of the sputtering gas. The TaN C (200) peak height increased first with the increase of nitrogen concentration, and then decreased with the further increase of the nitrogen concentration.[21]

Figure 1(b) shows that the as-deposited Mo–N sample had a hexagonal Mo_5N_6 crystal structure. After high-temperature N_2 annealing, it transformed to a cubic Mo_2N crystal structure. This structure was stable up to 800 °C N_2 annealing. Similarly, metallic Mo crystal phases were not observed in either as-deposited or annealed films. The change of the

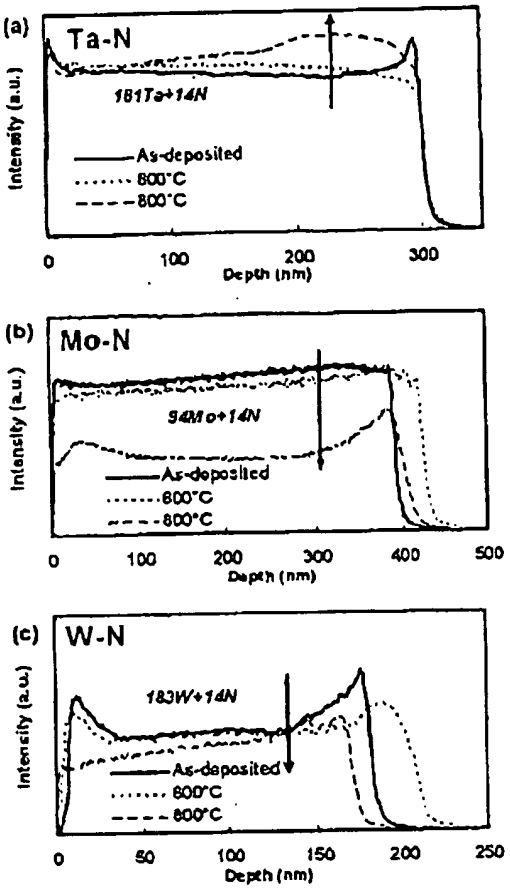

FIG. 2. SIMS depth profiles in clusters of composition as indicated for (a) tantalum nitride, (b) molybdenum nitride, and (c) tungsten nitride gate electrodes on 2.5 nm HfO_2 films with and without 10 s 600 or 800 °C N_2 annealing at 10 Torr. All the samples were also annealed in forming gas at 300 °C for 30 min after the backside Al deposition.

Mo/N ratio with the annealing temperature has been confirmed with SIMS analysis, as shown in Fig. 2(b). For the film after 800 °C N_2 annealing, further changes of crystal size or nitrogen concentration in the Mo–N films may occur, which leads to a sharp Mo_2N *C* (111) peak and a small Mo_2N *C* (200) peak. It was reported that the formation of either a two-phase structure (Mo_2N and Mo) or a single-phase structure (Mo_2N) was determined by the initial nitrogen concentration in the as-deposited MoN_x film.[22,23] The film's microstructure was insensitive to the process condition once the Mo_2N phase was formed. In this study, only the single-phase structure Mo_2N was detected after high-temperature N_2 annealing because the initial nitrogen concentration was high in the as-deposited film. A stable single-phase Mo_2N crystal structure was formed when the N_2 annealing temperature was as high as 800 °C.

Figure 1(c) shows that the as-deposited W–N film had a cubic W_2N crystal structure, which suggests that the as-deposited film was fully nitridized. The intensity of W_2N *C* (111) and *C* (200) peak heights increased with the N_2-annealing temperature. After 800 °C N_2 annealing, a small cubic W (110) peak appeared, which implies the formation of a metallic W phase. It was reported that the WN phase was not stable and a prominent W *C* (110) peak was detected after 1025 °C N_2 annealing.[24] The formation of a metallic W phase may be attributed to the dissociation of W–N or the crystallization of amorphous WN_x component in the film. For example, the amorphous metal-rich WN_x ($x \ll 0.5$) film tends to crystallize into W and W_2N phases at a relatively low temperature (~450 °C).[25] Since the $N_2/(Ar+N_2)$ ratio in the sputtering gas steam was very low (~2.5%), the as-deposited W–N gate should be metal-rich, and therefore, the formation of a metallic W phase after high temperature annealing is expected. Although the N-rich WN_x ($x > 1$) film is more stable and crystallizes at a higher temperature than the N-deficient WN_x film,[25] the film has a much higher resistivity and, therefore, is less desirable for gate electrode applications. It should be noted that the whole W–N system is complicated and a major effort is required to clear out all questions.[26] Since this topic is beyond the scope of this manuscript, authors could only identify the crystal structures before and after annealing from the XRD data shown in Fig. 1(c).

2. Nitrogen distributions in the bulk film and at the high-k interface

Both the nitrogen concentrations in the bulk metal nitride film and those across the nitride/HfO_2 interface are important parameters affecting electrical properties of the gate electrode as well as the MOS capacitor. Figure 2(a) shows the TOF-SIMS depth profile of Ta–N ion clusters in the as-deposited film and after 600 and 800 °C N_2-annealed films. The as-deposited film shows N piled up at the HfO_2 interface, which is due to the two-step deposition process. After 600 °C N_2 annealing, the nitrogen concentration in the bulk layer increased slightly, but the interface nitrogen concentration decreased. The decrease of the nitrogen concentration at the interface indicated that the original nitrogen atoms accumulated at the HfO_2 interface were weakly bonded, which could be removed by annealing at a moderate temperature. After 800 °C N_2 annealing, the nitrogen concentration further increased slightly in the bulk Ta–N film, but a large increase of nitrogen concentration occurred near the metal nitride/HfO_2 interface. This increase of nitrogen concentration may be attributed to the formation of N-rich Ta–N phase, e.g., Ta_3N_5, which was observed previously.[27] This N-rich Ta–N phase has a high resistivity and may lead to serious interaction between the Ta–N gate electrode and the underlying high-*k* layer, which will be discussed in later sections.

Figure 2(b) shows that the nitrogen concentration in the Mo–N film decreased after the high-temperature N_2 annealing step. The further decrease of nitrogen contents in the Mo–N gate electrodes after 800 °C annealing step compared to 600 °C annealing step implied that there could be some

extra nitrogen in the crystalline Mo_2N matrix, and the extra nitrogen could be lost during high-temperature annealing step. Figure 2(c) showing similar decreases of nitrogen concentrations were also observed in the W–N films. Schaeffer *et al.* also reported a similar reduction of the nitrogen level with increased annealing temperature based on the SIMS analysis.[24] For example, about a 20% nitrogen loss was observed after 800 and 900 °C annealing conditions; approximately 60% nitrogen loss was observed after 1025 °C annealing.

In this work, TOF-SIMS data mainly provided nitrogen composition profiles of both the bulk metal nitride film (200–400 nm) and the nitride/HfO_2 interface. X-ray diffraction provides the structure information of the bulk metal nitride film in the crystalline phase. The stoichiometry of the bulk metal nitride film in the crystalline phase can also be obtained by XRD analysis. Authors investigated the chemical composition change in the bulk nitride gate due to the N_2 thermal annealing process using the SIMS analysis. In addition, the stoichiometry change of the bulk nitride gate was studied using the XRD analysis. The SIMS result shows that the nitrogen concentration decreases in the bulk Mo–N and W–N gates after the N_2 annealing step, and the XRD result shows that the stoichiometry of the bulk Mo–N and W–N gates in the crystalline phase becomes nitrogen-deficient after the N_2 annealing step.

3. Metal nitride and HfO_2 interaction

One major problem of poly-Si gates is the reaction with the high-k layer to form an interface layer. The interaction between the metal nitride gate and high-k gate dielectric layer was investigated by TEM and EELS/EDXS. Figure 3(a) shows that the thickness of the as-deposited bulk high-k dielectric layer is around 2.2–2.5 nm. After 800 °C N_2 annealing, the thicknesses of the bulk high-k dielectric layer drastically increased to 3.0–3.2 nm when Ta–N was used as the gate electrode, as shown in Fig. 3(b). This increase of the high-k dielectric layer thickness could be related to the increase of the nitrogen concentration, as shown in the TOF-SIMS profile of Fig. 2(a). However, the thicknesses of the bulk high-k dielectric layer only increased to 2.5–2.7 nm when Mo–N and W–N were used as the gate electrodes, as shown in Figs. 3(c) and 3(d).

Figure 4(a) shows the EELS profiles of O, N, and Si across the Ta–N/HfO_2 dielectric interface region. There is an apparent overlap between the O and N element profiles at the top interface region. Figure 4(b) shows EDXS profiles of the same sample, which also confirms the overlap of the Hf and Ta element profiles. The element profiles in Figs. 4(a) and 4(b) suggest that a top interface layer containing Ta, Hf, O, and N atoms was formed at the Ta–N/HfO_2 contact area after 800 °C N_2 annealing. Since this interface layer contains metal atoms, i.e., Hf and Ta, with similar sizes and atomic weights, it is difficult to differentiate this interface layer from the bulk HfO_2 film in the HRTEM image. Therefore, the thick high-k gate dielectric layer as shown in the HRTEM image may be contributed by both the top interface layer and the remaining bulk HfO_2 layer.

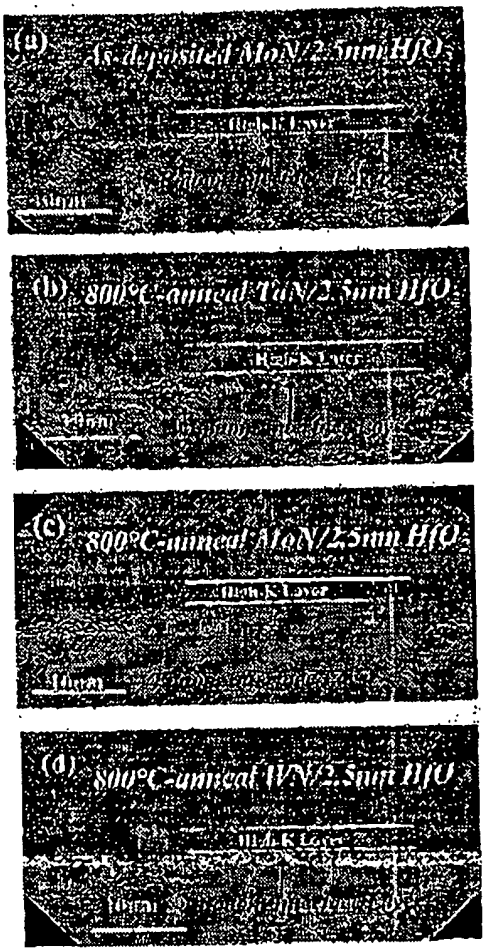

FIG. 3. Comparison of high resolution TEM image of (a) as-deposited Mo–N/2.5 nm HfO_2/Si stack, (b) 800 °C N_2-annealed Ta–N/2.5 nm HfO_2/Si, (c) 800 °C N_2-annealed Mo–N/2.5 nm HfO_2/Si, (d) 800 °C N_2-annealed W–N/2.5 nm HfO_2/Si stack structures. All the samples were also annealed in forming gas at 300 °C for 30 min after the backside Al deposition.

Although similar overlaps between the O and N element profiles were detected by EELS on Mo–N/HfO_2/Si and W–N/HfO_2/Si gate stack structures, the details were different. For example, overlap between the O and N element profiles in the Ta–N gate electrode sample was much more serious and apparent than that in the Mo–N or W–N gate electrode sample. The O shoulder stretched wider toward the metal gate area in the sample with Ta–N gate electrode but relatively less in samples with Mo–N or W–N gate electrode. HRTEM results also showed no dramatic increase of the bulk high-k gate dielectric thickness in these two stack structures. Therefore, no serious interaction occurred at the

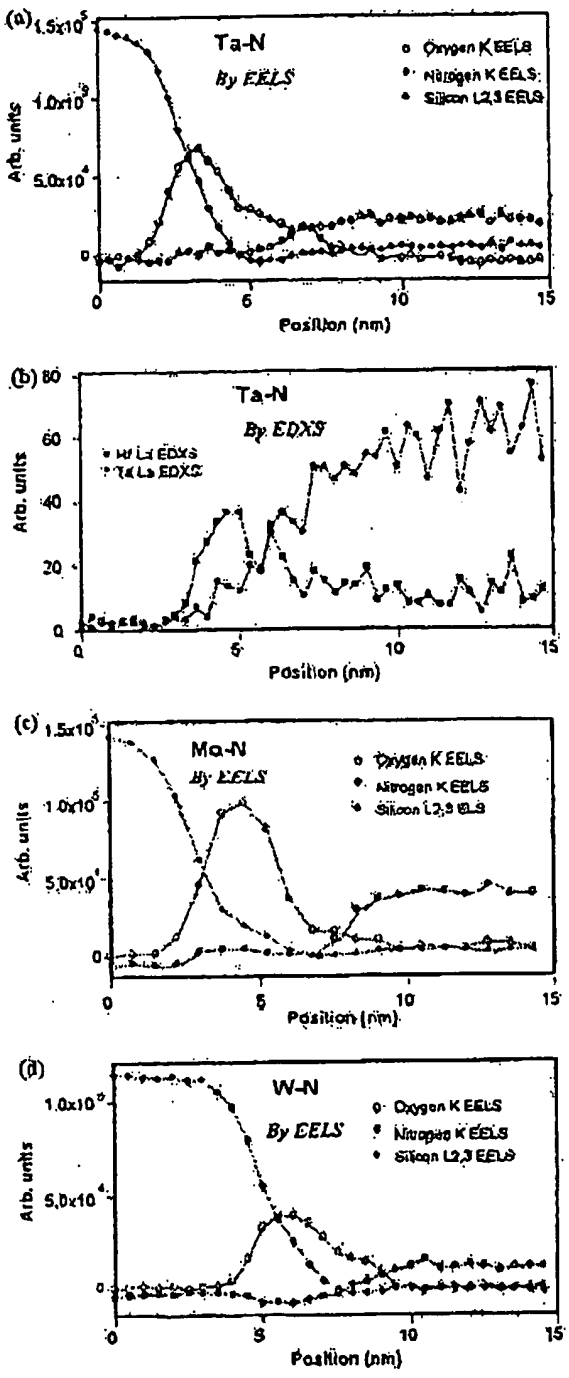

FIG. 4. (a) EELS and (b) EDXS profiles of 800 °C N_2-annealed Ta–N/2.5 nm HfO_2/Si stack structures. (c) EELS profiles of 800 °C N_2-annealed Mo–N/2.5 nm HfO_2/Si stack structures. (d) EELS profiles of 800 °C N_2-annealed W–N/2.5 nm HfO_2/Si stack structures. All the samples were also annealed in forming gas at 300 °C for 30 min after the backside Al deposition.

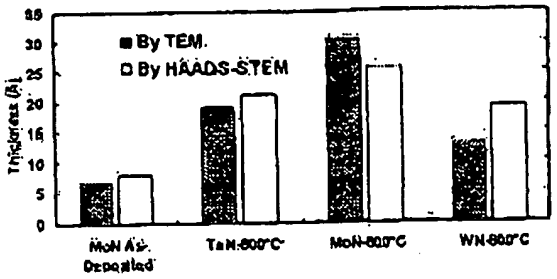

FIG. 5. Bottom interface layer thickness for different gate electrodes with and without 800 °C N_2 annealing. All the samples were also annealed in forming gas at 300 °C for 30 min after the backside Al deposition.

Mo–N/HfO_2 or W–N/HfO_2 interface after 800 °C N_2 annealing step. In this study, among the three metal nitride gate electrodes, Ta–N is least stable because it reacted with N_2 and HfO_2 at a high N_2 annealing temperature. Other researchers also reported similar results, e.g., there was some interdiffusion between Hf and Ta atoms after 1025 °C, but no Hf and W interdiffusion was reported at the same temperature.[24] These results may be contributed by the similarities between Ta and Hf atoms in terms of the weight, electronegativity, and radii.[28]

4. Metal nitride gate influence on the bottom HfO_2 and Si interface layer

An approximately 0.6-nm-thick bottom interface layer was formed at HfO_2/Si interface for the as-deposited Mo–N/2.5 nm HfO_2/Si stack, as shown in Fig. 3(a). An increase of the bottom interface layer thickness was observed for all three metal nitride gate/HfO_2/Si stacks after 800 °C N_2 annealing, as shown in Figs. 3(b)–3(d). The bottom interface layer thicknesses could also be estimated from the inflection point of the high-angle annular dark-field imaging (HAADF)-scanning transmission electron microscopy (STEM) image intensity profiles (not shown here).[29,30] Figure 5 is a summary of the bottom interface thickness measured from TEM and HAADF-STEM of all three metal gate samples after 800 °C N_2 annealing step. The bottom interface layer thicknesses estimated by the two methods show similar trends about the effect of 800 °C N_2 annealing step on the bottom interface layer thickness. For example, after 800 °C N_2 annealing, the bottom interface layer thickness increases substantially for all three gate stack structures. Different gate electrodes affect the bottom interface layer thickness differently. Other researchers also reported that the gate electrode materials have some impact on the formation of the bottom interface layer.[24,31] This may be attributed to the difference in the oxygen-block capabilities of various gate electrode materials at high temperature.[31] However, since the postmetal annealing steps were performed in either an ultrahigh-purity, e.g., 99.999%, N_2 or N_2/H_2 forming gas ambient and there was almost no oxygen, e.g., <1 ppm, present in the annealing ambient, the introduction of oxygen from the environment during the annealing steps can be ne-

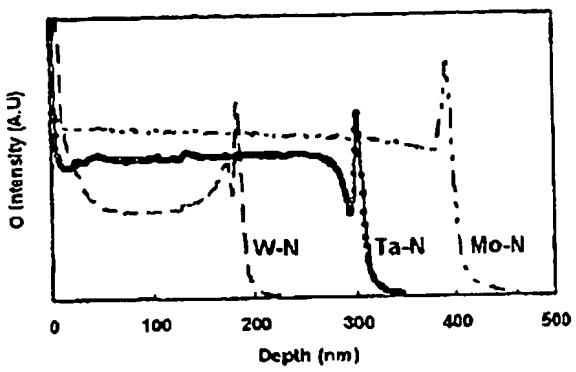

FIG. 6. SIMS depth profiles of oxygen impurity in the as-deposited metal nitride gate electrodes.

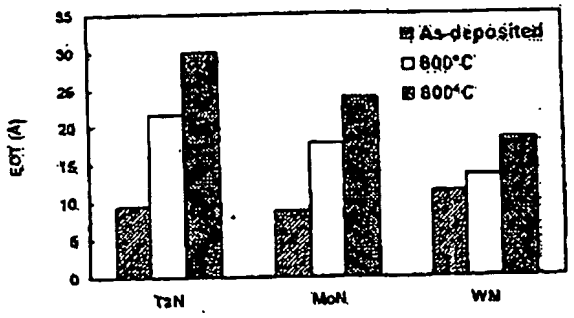

FIG. 7. EOT variance with N_2 annealing treatments for samples with different gate electrodes.

glected. There must be some other reasons for the increase of the bottom interface layer thickness. Figure 6 shows that the oxygen impurity concentration in the as-deposited Mo–N gate electrode was the highest among all three gate electrodes, which is consistent with its thickest bottom interface layer after 800 °C N_2 annealing. The lowest oxygen concentration was detected in the as-deposited W–N gate electrode, which had the thinnest bottom interface layer after 800 °C N_2 annealing. Based on this observation, a possible contribution factor for the increase of the bottom interface layer thickness is the existing oxygen in the as-deposited film, which may diffuse at high annealing temperatures. However, this mechanism needs further studies. The high oxygen concentration in the Mo–N film may come from the target. A more detailed analysis of the target is required to verify the above assumption. Results in this section suggest that any possible oxygen source in the process should be eliminated in order to reduce the bottom interface layer thickness.

B. Electrical properties

1. Resistivity

Table I shows the resistivity of three metal nitride gate electrodes with different N_2 annealing temperatures. For as-deposited films, low resistivity (~50–70 $\mu\Omega$ cm) was achieved for all three gate electrode materials. However, the Ta–N gate electrode shows a sharp increase of resistivity after 800 °C N_2 annealing. It was reported that the as-deposited TaN_x films with relatively high nitrogen concentration would have relatively low thermal stability in terms of resistivity.[32] The sharp increase of resistivity after a high-temperature annealing can be attributed to the formation of an N-rich Ta–N phase, such as Ta_3N_5.[24,27] In this study, SIMS analyses indicated an increase of nitrogen content in the TaN gate electrode after 800 °C N_2 annealing as shown in Fig. 2(a), but no crystalline N-rich Ta–N structure was observed in the XRD patterns. The N-rich Ta–N phase may still be in amorphous phase. Tantalum nitride has many polymorphs and their properties vary depending on the nitrogen contents.[33]

TABLE I. Resistivity of metal gate electrodes on HfO_2 films with different high-temperature N_2 annealing conditions. All the samples were also annealed in forming gas at 300 °C for 30 min after the backside Al deposition.

Gate electrodes	As-deposited ($\mu\Omega$ cm)	600 °C N_2 anneal ($\mu\Omega$ cm)	800 °C N_2 anneal ($\mu\Omega$ cm)
Ta–N	70	80	5000
Mo–N	60	48	48
W–N	50	36	36

The Mo–N and W–N gate electrodes show a relatively stable resistivity up to 800 °C N_2 annealing. A slight decrease of resistivity was observed for both gate electrode materials. This observation is consistent with the slight nitrogen loss after high-temperature N_2 annealing as shown in the SIMS profiles. The decrease of resistivity may also be attributed to the grain growth of the Mo–N and W–N gate electrodes after the high-temperature N_2 annealing, as shown in Figs. 1(b) and 1(c).

2. Equivalent oxide thickness

Figure 7 shows the equivalent oxide thicknesses (EOTs) of Ta–N, Mo–N, and W–N gate electrodes/2.5 nm HfO_2 MOS capacitors at different N_2 annealing temperatures. Low EOTs (0.9–1.1 nm) were achieved for the as-deposited samples. The EOT increased unanimously with the N_2 annealing temperature. The EOT increase can be attributed to the increase of the bottom interface layer thickness as shown in previous TEM results. The largest EOT (~3.0 nm) was observed for samples with the Ta–N gate electrode after 800 °C N_2 annealing. This can be explained by the formation of a thick top interface as a result of serious interaction between the Ta–N electrode and the HfO_2 film. The sample with the Mo–N gate electrode also shows a large EOT (~2.4 nm) after 800 °C N_2 annealing, which can be explained by the dramatic increase of the bottom interface layer thickness as shown in the TEM figure. Samples with the W–N gate electrode display a relatively small variation of EOT after high-temperature N_2 annealing, which is consistent with the TEM result shown in Fig. 3.

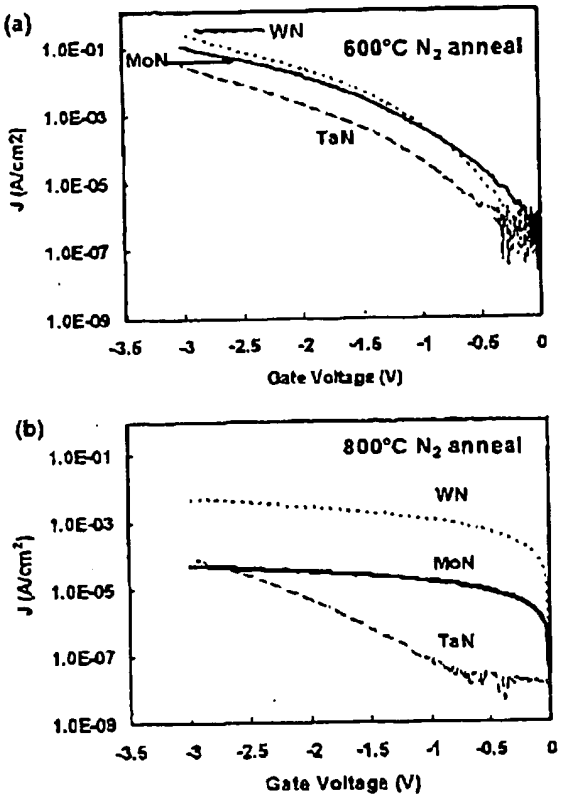

FIG. 8. Comparison of leakage current densities for samples with different gate electrodes after (a) 600 °C N_2 annealing and (b) 800 °C N_2 annealing.

3. Leakage current density

Figure 8 shows the leakage current density (J) versus gate voltage (V) curves of capacitors with different metal nitride gates after (a) 600 °C and (b) 800 °C N_2 annealings. The 800 °C N_2 annealing samples show lower leakage current densities than 600 °C N_2 annealing samples. The decrease of the leakage current densities can be explained by the increase of EOT. The EOT value is contributed by both the bulk high-k and the interface layers. In addition to the film thickness, material properties of each layer, such as the composition and density, also affect the leakage current mechanism. Samples with the Ta–N gate electrode always show the lowest leakage current densities among the three types of samples. This is consistent with its large EOT value. However, for the 800 °C N_2-annealed sample with the Ta–N gate electrode, the leakage current is three orders of magnitude lower than that of the 600 °C N_2-annealed sample. The decrease of the leakage current density cannot be solely explained by the slight increase of EOT, i.e., 0.8 nm. The low leakage current could also be contributed by material property changes of the bulk high-k and interface layers. For example, Figures 4(a) and 4(b) showed a serious interaction between Ta–N and HfO_2, which resulted in the formation of a top interface layer containing Ta, Hf, O, and N atoms. It was reported that the formation of an oxynitride interface layer would reduce the leakage current density of the high-k gate stack structure.[34,35]

The leakage current of the 800 °C N_2-annealed sample with the W–N gate electrode is about two orders of magnitude higher than that of the sample with the same N_2 annealing temperature but with Mo–N gate electrode. However, the EOT of the former is only 0.6 nm lower than that of the latter. Therefore, other factors might contribute to the unusual high leakage current. One possible reason is the formation of a metallic W phase in the W–N film, as shown in the Fig. 1(c). It was reported that, for the same high-k gate dielectric films, a WN_x gate electrode showed a lower leakage current density than the W gate electrode.[36,37] WN_x is superior to W as a gate electrode because the nitrogen from WN_x can be incorporated into the high-k film. The metallic W in the W–N electrode may change the metal gate/high-k top interface properties or even penetrate the high-k film to create a leaky path, which results in a high leakage current density.

4. Gate electrode work functions

The work functions (Φ_m) of the metal nitride gate electrode was extracted from the plots of flatband voltage (V_{FB}) versus EOT.[24,38] In this study, a simple linear relation between V_{FB} and EOT was assumed,

$$V_{FB} = \Phi_{ms} \pm \frac{Q_{eff}\mathrm{EOT}}{\varepsilon_{SiO_2}}, \tag{1}$$

where Q_{eff} is the effective oxide charge at the oxide interface, ε_{SiO_2} is the permittivity of SiO_2 (3.45×10^{-13} F/cm), and Φ_{ms} is the difference between the electrode work function (Φ_m) and Si substrate (p type $\sim10^{17}$ cm^{-3} doping level) work function ($\Phi_s \sim 5.09$ eV). The plus and minus ($\pm$) sign represents the positive and negative fixed charges, respectively. The Q_{eff} and the Φ_{ms} can be extracted from the slope and intercepts of the V_{FB} vs EOT plot, respectively. The linear relationship in Eq. (1) is only a simple model traditionally used to extract the work function assuming that the stacked high k is a homogeneous layer. However, since the high-k stack is composed of two distinct layers, for more accurate characterization of the work function and charge densities, a large array of samples, such as different SiO_2 interface layer and bulk high-k thicknesses, needs to be prepared.[39] Currently, authors are working on these samples. The result will be published in a separate paper.

According to calculations of Eq. (1), the ϕ_M of Ta–N, Mo–N, and W–N after 600 °C N_2 annealing are about 5.0, 4.5, and 4.29 eV, respectively. For films after 800 °C N_2 annealing, the ϕ_M of Ta–N, Mo–N, and W–N decreased to 4.23, 4.16, and 4.06 eV, respectively. The work functions of all three gate electrode materials are suitable for n-type metal-oxide-semiconductor (NMOS) application after 800 °C N_2 annealing.[9,24] For the Ta–N gate electrode, a drastic change of work function after 800 °C N_2 annealing was observed, which is due to its poor thermal stability and serious interaction with the HfO_2. The TEM, EELS, and SIMS

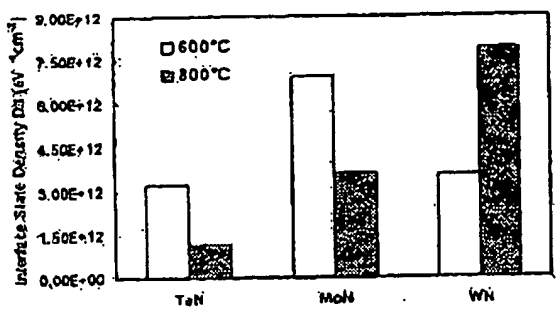

FIG. 9. N_2 annealing temperature effects on the interface state density (D_{it}) for samples with different gate electrodes.

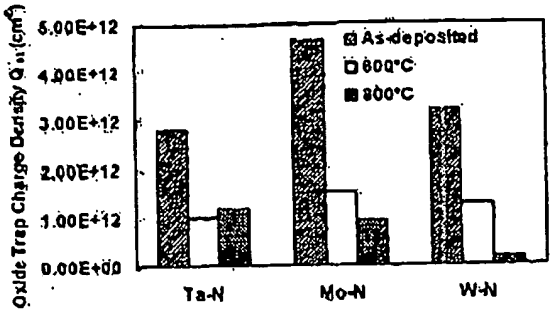

FIG. 10. Oxide trap charge density (Q_{ot}) of samples with different gate electrodes.

results confirm the serious interaction at the Ta–N and HfO_2 interface after 800 °C N_2 annealing. The small variation of the work functions of Mo–N and W–N gate electrodes between 600 and 800 °C N_2 annealing conditions can be explained by the minor changes of microstructures and chemical compositions as shown in XRD and SIMS results. The change of work function after thermal treatment had been observed by many other researchers.[24,40] Crystallization, structure, and chemical composition can affect the work function of the metal gate electrodes above the HfO_2 films.[24,40] In this study, the change of work function can be related to the changes of the physical properties of metal nitride gate electrodes after high-temperature treatment.

5. Interface state density

Figure 9 shows the change of interface state density (D_{it}) of 2.5 nm HfO_2 films with different N_2 annealing temperatures. The D_{it} in this work was extracted at the midgap by the single frequency approximation method (Hill's method) from 1 MHz/100 kHz frequency C-V measurement.[41] For the samples with Ta–N and Mo–N gate electrodes, the D_{it} decreased with the increase of the N_2 annealing temperature. This suggested that the high-temperature N_2 annealing step can be effective in annealing out the damage caused by the PVD gate deposition process.[42,43]

However, samples with W–N gate electrodes show a different trend on the change of D_{it} after 800 °C N_2 annealing. The 800 °C N_2-annealed sample has a slightly higher D_{it} than the 600 °C N_2-annealed sample. This phenomenon has been observed on Ta_2O_5 high-k films and the W/WN gate electrode.[42] The exact reason for the increase of D_{it} after high-temperature annealing is still unknown. In this study, the increase of D_{it} for W–N gate may be attributed to the formation of the metallic W phase in the W–N gate electrodes after 800 °C N_2 annealing, which was close to the bottom high-k/Si interface and degraded the interface quality.

It should be noticed that the D_{it} value is also influenced by the metal gate electrode material. For example, samples with a Ta–N gate show a lower D_{it} value than those with the other two gate electrode materials regardless of the N_2 annealing temperature. The gate electrode material and metal gate deposition conditions were reported to affect the interface state density of MOS with SiO_2 and high-k gate dielectrics.[27,42,43] There are several possible explanations. For example, some deposition processes may cause more damages to the thin gate dielectric film than other processes, e.g., high ion bombard energy or strong short-wavelength light radiation during sputtering. In addition, different gate electrodes may have different stresses, which could affect the interface state density.[44] Another reason may be associated with the different barrier properties of metal gate electrodes related to the diffusion of hydrogen atoms during the post metal forming gas annealing step. More detailed studies on the gate electrode effects on the interface state density are under progress.

6. Oxide trap charge density

Figure 10 shows the bulk oxide trap charge density (Q_{ot}) of 2.5 nm HfO_2 films with different metal nitride gate electrode materials. The Q_{ot} was extracted from the hysteresis of the C-V curves using the following equation:

$$Q_{ot} = -\frac{C_{ox}\Delta V_{FB}}{q}, \tag{2}$$

where the ΔV_{FB} is the flatband voltage shift after a forward-and-reverse voltage sweep from −3 to +3 V, q is the electronic charge, and C_{ox} is the accumulation capacitance per unit area. Figure 10 shows that in all cases the Q_{ot} value decreases after the high-temperature N_2 annealing step. High-temperature annealing can effectively reduce defects in the high-k film caused by the sputter deposition process of the gate electrode. In addition, after N_2 annealing, the overall high-k stack physical thickness increased. Under the same sweep voltage condition, the effective electrical field and the amount of the injected charges decreased accordingly, which may also lead to a lower Q_{ot}. For samples with W–N and Mo–N gate electrodes, a lower Q_{ot} was achieved by increasing the N_2 annealing temperature, e.g., from 600 to 800 °C. The lowest Q_{ot} was obtained for the sample with a W–N gate electrode after 800 °C N_2 annealing. However, a slight increase of Q_{ot} was observed for the sample with the Ta–N gate electrode after 800 °C N_2 annealing compared to the

sample after 600 °C N_2 annealing. This can be explained by the serious interaction between the TaN and HfO_2 film after 800 °C N_2 annealing. EELS result in Figs. 4(a) and 4(b) showed that a top interface layer containing Ta, Hf, O, and N atoms was formed at the Ta–N/HfO_2 contact region, which increased the oxide trap density of the high-k gate stack structure.[45,46]

IV. CONCLUSIONS

Ta–N, Mo–N, and W–N were investigated as gate electrodes for a 2.5-nm-thick HfO_2 high-k dielectric material. Their physical and electrical properties were affected by the high-temperature N_2 annealing treatment conditions. Serious interaction was observed at the Ta-N/HfO_2 interface after 800 °C N_2 annealing, and a top interface layer containing Ta, Hf, O, and N atoms was formed, which lead to an increase of EOT and bulk charge trap density. No significant interaction occurred at the W–N/HfO_2 or Mo–N/HfO_2 interface. The metallic W was formed after 800 °C N_2 annealing, which lead to a high leakage current density. The gate electrode material also affected the bottom interface's electrical properties. A thick bottom interface layer was formed at the HfO_2/Si interface for the sample with a Mo–N gate electrode, which lead to a high EOT after a high-temperature N_2 annealing. Work functions of these three gate electrodes are suitable for NMOS applications after 800 °C N_2 annealing. In summary, metal nitrides can be used as the gate electrode materials for the HfO_2 high-k film. However, when interpreting electrical properties, the deposition and after-deposition process conditions have to be specified carefully.

ACKNOWLEDGMENTS

This research was partially supported by NSF Project No. ECS-0403280 and SEMATECH Contract No. 309366. The authors thank Dr. B. Foran of SEMATECH for TEM, EELS, EDXS, and SIMS analyses. Dr. P. Majhi of SEMATECH is acknowledged for supplying ALD HfO_2 samples and technical discussions.

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- Typical Granulations Available:

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Density (g/cm³)	17.8
Specific Gravity	
Specific Heat @25°C (cal/g-°C)	
Melting Point (°C)	
Boiling Point (°C)	

Surface Area (m^2/g)	
Thermal Conductivity @20°C (cal/s-cm-°C)	
Mohs Hardness @20°C	
pH	
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Color	

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